CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method, comprising:

creating a first descriptor to correspond to a first data block; and

placing the first descriptor in a descriptor ring according to a striping policy to prevent false sharing of a cache line between a plurality of processors of [[the]] a computer system, wherein the striping policy assigns a first processor of the plurality of processors to the first descriptor according the following relationship:

Processor Assignment = Descriptor_Position mod N,

where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors.

2. (Currently Amended) The method of claim 1 wherein the striping policy comprises placing the first descriptor in the descriptor ring ~~wherein~~ such that the first descriptor and a second descriptor in the descriptor ring [[to]] do not share the cache line when the second descriptor is requested, wherein the first descriptor to be the next descriptor requested from the descriptor ring after the second descriptor.

3. (Cancelled)

4. (Currently Amended) The method of claim 1 ~~wherein the plurality of processors share a cache line,~~ wherein the cache line is longer than the first descriptor.

5. (Original) The method of claim 4 wherein the cache line is 64 bytes long and the first descriptor is 16 bytes long.

6. (Currently Amended) The method of claim 1 further comprising receiving ~~wherein~~ the first data block ~~to be received~~ at an I/O device of the computer system from external to the computer system.

7. (Currently Amended) The method of claim 1 wherein the first data block is prepared at the computer system to be sent to [[the]] an I/O device of the computer system.

8. (Currently Amended) An article of manufacture comprising:

a machine-readable medium including a plurality of instructions which when executed perform operations comprising:

allocating a first receive buffer at a computer system including a plurality of processors, the first receive buffer to store a first packet received at a network interface card (NIC) of the computer system;

creating a first descriptor corresponding to the first receive buffer; and

placing the first descriptor in a descriptor ring according to a striping policy to prevent false sharing between the plurality of processors of a cache line of the computer system, wherein the striping policy assigns a first processor of the plurality of processors to the first descriptor according the following relationship:

Processor Assignment = Descriptor_Position mod N,

where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors.

9. (Currently Amended) The article of manufacture of claim 8 wherein the striping policy comprises placing the first descriptor in the descriptor ring ~~wherein~~ such that the first descriptor and a second descriptor in the descriptor ring [[to]] do not share the cache line when the second descriptor is requested, the first descriptor to be the next descriptor requested from the descriptor ring after the second descriptor.

10. (Cancelled)

11. (Original) The article of manufacture of claim 8 wherein the plurality of instructions are embodied in a NIC device driver associated with the NIC.

12. (Currently Amended) The article of manufacture comprising:

a machine-readable medium including a plurality of instructions which when executed perform operations comprising:

creating a first descriptor at a computer system including a plurality of processors, the first descriptor to correspond to a first packet to be transmitted by a network interface card (NIC) of the computer system; and

placing the first descriptor in a descriptor ring according to a striping policy to prevent false sharing of a cache line between the plurality of processors of the computer system, wherein the striping policy assigns a first processor of the plurality of processors to the first descriptor according the following relationship:

Processor Assignment = Descriptor_Position mod N,

where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors.

13. (Original) The article of manufacture of claim 12 wherein the striping policy comprises placing the first descriptor in the descriptor ring wherein the first descriptor and a second descriptor in the descriptor ring to not share the cache line when the second descriptor is requested, the first descriptor to be the next descriptor requested from the descriptor ring after the second descriptor.

14. (Cancelled)

15. (Original) The article of manufacture of claim 12 wherein the plurality of instructions are embodied in a NIC device driver associated with the NIC.

16. (Currently Amended) A computer system, comprising:

a plurality of network interface cards (NICs);

a plurality of processors, each of the plurality of processors communicatively coupled to each of the plurality of NICs; and

a storage device operatively coupled to the plurality of processors, the storage device including a plurality of instructions which when executed by a processor of the plurality of processors perform operations comprising:

creating a first descriptor to correspond to a first packet; and

placing the first descriptor in a descriptor ring according to a striping policy to prevent false sharing of a cache line between the plurality of processors of the computer system, wherein the striping policy assigns a first processor of the plurality of processors to the first descriptor according the following relationship:

Processor Assignment = Descriptor_Position mod N,

where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors.

17. (Original) The computer system of claim 16 wherein the striping policy comprises placing the first descriptor in the descriptor ring wherein the first descriptor and a second descriptor in the descriptor ring to not share the cache line when the second descriptor is requested, the first descriptor to be the next descriptor requested from the descriptor ring after the second descriptor.

18. (Cancelled)

19. (Original) The computer system of claim 16 wherein execution of the plurality of instructions further perform operations comprising receiving the first packet at a NIC of the plurality of NICs.

20. (Original) The computer system of claim 16 wherein execution of the plurality of instructions further perform operations comprising preparing the first packet at the computer system, the first packet to be transmitted from a NIC of the plurality of NICs.